Λύση 2ης άσκησης

Αλγόριθμος Tomasulo χωρίς ROB

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1				

	Busy	Address
Load1		
Load2		
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1			
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 1

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1						
	Add2						
	Add3						
	Add4						
	Mul1						
	Mul2						
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi					

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2			
SUB.D	F0	F0	F2	2				

	Busy	Address
Load1		
Load2		
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1			
Store2			
Store3			
Store4			
Store5			

```
foo: L.D     F0   0(R1)
     SUB.D   F0   F0    F2
     DIV.D   F2   F2    F0
     L.D     F0   8(R1)
     DIV.D   F4   F0    F6
     S.D     F4   16(R1)
     DADDI   R1   R1    #-24
     BNEZ    R1   foo
```

Clock: 2

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1						
	Add2						
	Add3						
	Add4						
	Mul1						
	Mul2						
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi					

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3		
SUB.D	F0	F0	F2	2	3			
DIV.D	F2	F2	F0	3				

	Busy	Address
Load1	Yes	M[0+R1]
Load2		
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1			
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock: 3

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1						
	Add2						
	Add3						
	Add4						
	Mul1						
	Mul2						
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Load1				

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4	
SUB.D	F0	F0	F2	2	3	4		
DIV.D	F2	F2	F0	3	4			
L.D	F0	8	R1	4				

	Busy	Address
Load1	Yes	M[0+R1]
Load2		
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1			
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock
4

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	Yes	sub.d		R[F2]	Load1	
	Add2						
	Add3						
	Add4						
	Mul1						
	Mul2						
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

- WAW hazard μεταξύ L.D/SUB.D:
ο F0 μετονομάζεται σε “Add1”

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Add1				

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4		
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5			
DIV.D	F4	F0	F6	5				

	Busy	Address
Load1	No	
Load2		
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1			
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 5

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
5	**Add1**	Yes	sub.d	M[0+R1]	R[F2]		
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]			Add1
	Mul2						
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Add1	Mul1			

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6	
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6		
DIV.D	F4	F0	F6	5	6			
S.D	F4	16	R1	6				

	Busy	Address
Load1	No	
Load2	Yes	M[8+R1]
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1			
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 6

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
4	**Add1**	Yes	sub.d	M[0+R1]	R[F2]		
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]			Add1
	Mul2						
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

- WAW hazard μεταξύ SUB.D/L.D:
ο F0 μετονομάζεται σε “Load2”

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Load2	Mul1			

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6	
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7	
DIV.D	F4	F0	F6	5	6	7		
S.D	F4	16	R1	6	7			
DADDI	R1	R1	#-24	7				

	Busy	Address
Load1	No	
Load2	Yes	M[8+R1]
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1			
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 7

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
3	**Add1**	Yes	sub.d	M[0+R1]	R[F2]		
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]			Add1
	Mul2	Yes	div.d		R[F6]	Load2	
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Load2	Mul1	Mul2		

Instruction		j	k
L.D	F0	0	R1
SUB.D	F0	F0	F2
DIV.D	F2	F2	F0
L.D	F0	8	R1
DIV.D	F4	F0	F6
S.D	F4	16	R1
DADDI	R1	R1	#-24
BNEZ	R1	foo	

IF	ID	IS	EX	WB
1	2	3	4 – 4	5
2	3	4	6	
3	4	5		
4	5	6	7 – 7	8
5	6	7		
6	7	8		
7	8			
8				

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock: 8

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
2	**Add1**	Yes	sub.d	M[0+R1]	R[F2]		
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]			Add1
15	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3						
	Mul4						
	Int1						
	Int2						
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6	
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9		
BNEZ	R1	foo		8	9			

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Res. Stations

Clock	Time	Name	Busy	Op	Vj	Vk	Qj	Qk
9	1	**Add1**	Yes	sub.d	M[0+R1]	R[F2]		
		Add2						
		Add3						
		Add4						
		Mul1	Yes	div.d	R[F2]			Add1
	14	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
		Mul3						
		Mul4						
		Int1	Yes	daddi	R[R1]	#-24		
		Int2						
		Int3						
		Int4						
		Int5						

- δεν υπάρχει πρόβλεψη διακλάδωσης, άρα δεν φορτώνεται η επόμενη εντολή

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		Int1

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10	
BNEZ	R1	foo		8	9	10		

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 10

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
0	**Add1**	Yes	sub.d	M[0+R1]	R[F2]		
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]			Add1
13	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3						
	Mul4						
	Int1	Yes	daddi	R[R1]	#-24		
	Int2	Yes	bnez			Int1	
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		Int1

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	
BNEZ	R1	foo		8	9	10		

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Res. Stations

Clock	Time	Name	Busy	Op	Vj	Vk	Qj	Qk
11		**Add1**	No					
		Add2						
		Add3						
		Add4						
		Mul1	Yes	div.d	R[F2]	R[F0]		
	12	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
		Mul3						
		Mul4						
		Int1	Yes	daddi	R[R1]	#-24		
		Int2	Yes	bnez			Int1	
		Int3						
		Int4						
		Int5						

- conflict στο CDB μεταξύ SUB.D/DADDI

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		Int1

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10		

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Res. Stations

Clock 12

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
11	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3						
	Mul4						
	Int1	No					
	Int2	Yes	bnez	R[R1]			
	Int3						
	Int4						
	Int5						

- η 1η div δεν μπορεί να αρχίσει διότι η μονάδα είναι κατειλημμένη

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13	

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 13

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
10	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3						
	Mul4						
	Int1	No					
	Int2	Yes	bnez	R[R1]			
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14				

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Res. Stations

Clock 14

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
9	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3						
	Mul4						
	Int1	No					
	Int2	No					
	Int3						
	Int4						
	Int5						

- έγινε γνωστό το αποτέλεσμα της BNEZ, άρα μπορούμε να φορτώσουμε την επόμενη εντολή

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15			
SUB.D	F0	F0	F2	15				

	Busy	Address
Load1	No	
Load2	No	
Load3		
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 15

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
8	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3						
	Mul4						
	Int1	No					
	Int2	No					
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul1	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16		
SUB.D	F0	F0	F2	15	16			
DIV.D	F2	F2	F0	16				

	Busy	Address
Load1	No	
Load2	No	
Load3	Yes	M[0+R1]
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 16

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2						
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
7	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3						
	Mul4						
	Int1	No					
	Int2	No					
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Load3	Mul1	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17	
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17			
L.D	F0	8	R1	17				

	Busy	Address
Load1	No	
Load2	No	
Load3	Yes	M[0+R1]
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Res. Stations

Clock	Time	Name	Busy	Op	Vj	Vk	Qj	Qk
17		**Add1**	No					
		Add2	Yes	sub.d			Load3	Mul1
		Add3						
		Add4						
		Mul1	Yes	div.d	R[F2]	R[F0]		
	6	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
		Mul3						
		Mul4						
		Int1	No					
		Int2	No					
		Int3						
		Int4						
		Int5						

- WAW hazard μεταξύ L.D/SUB.D:
ο F0 μετονομάζεται σε “Add2”

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Add2	Mul1	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18			
DIV.D	F4	F0	F6	18				

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4		
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Res. Stations

Clock 18

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
5	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3	Yes	div.d			Mul1	Add2
	Mul4						
	Int1	No					
	Int2	No					
	Int3						
	Int4						
	Int5						

- WAW hazard μεταξύ 1ης/3ης DIV.D:
ο F2 μετονομάζεται σε “Mul3”

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Add2	Mul3	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19		
DIV.D	F4	F0	F6	18	19			
S.D	F4	16	R1	19				

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	Yes	M[8+R1]
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 19

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
4	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3	Yes	div.d			Mul1	Add2
	Mul4						
	Int1	No					
	Int2	No					
	Int3						
	Int4						
	Int5						

- WAW hazard μεταξύ 4ης L.D/2ης SUB.D:
ο F0 μετονομάζεται σε “Load4”

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Load4	Mul3	Mul2		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20	
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20			
DADDI	R1	R1	#-24	20				

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	Yes	M[8+R1]
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2			
Store3			
Store4			
Store5			

```
foo: L.D    F0    0(R1)
     SUB.D  F0    F0     F2
     DIV.D  F2    F2     F0
     L.D    F0    8(R1)
     DIV.D  F4    F0     F6
     S.D    F4    16(R1)
     DADDI  R1    R1     #-24
     BNEZ   R1    foo
```

Res. Stations

Clock 20

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
3	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d		R[F6]	Load4	
	Int1	No					
	Int2	No					
	Int3						
	Int4						
	Int5						

- WAW hazard μεταξύ 2ης/4ης DIV/D:
ο F4 μετονομάζεται σε “Mul4”

Reg. res.status

	F0	F2	F4	F6	R1
Qi	Load4	Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21			
BNEZ	R1	foo		21				

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0    0(R1)
     SUB.D  F0    F0    F2
     DIV.D  F2    F2    F0
     L.D    F0    8(R1)
     DIV.D  F4    F0    F6
     S.D    F4    16(R1)
     DADDI  R1    R1    #-24
     BNEZ   R1    foo
```

Clock 21

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
2	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3						
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22		
BNEZ	R1	foo		21	22			

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 22

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
1	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	Yes	daddi	R[R1]	#-24		
	Int4						
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		Int3

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5		
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23	
BNEZ	R1	foo		21	22	23		

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	Mul2
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

foo:	L.D	F0	0(R1)	
	SUB.D	F0	F0	F2
	DIV.D	F2	F2	F0
	L.D	F0	8(R1)	
	DIV.D	F4	F0	F6
	S.D	F4	16(R1)	
	DADDI	R1	R1	#-24
	BNEZ	R1	foo	

Clock
23

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
	Mul1	Yes	div.d	R[F2]	R[F0]		
0	**Mul2**	Yes	div.d	M[8+R1]	R[F6]		
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	Yes	daddi	R[R1]	#-24		
	Int4	Yes	bnez			Int3	
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		Int3

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24	
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8		
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	
BNEZ	R1	foo		21	22	23		

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 24

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
14	**Mul1**	Yes	div.d	R[F2]	R[F0]		
	Mul2	No					
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	Yes	daddi	R[R1]	#-24		
	Int4	Yes	bnez			Int3	
	Int5						

- CDB conflict ανάμεσα σε DIV.D/DDADI
- η 1η DIV αρχίζει την εκτέλεση

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		Int3

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24	
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25	
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23		

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	Yes	M[16+R1]	
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

foo:	L.D	F0	0(R1)	
	SUB.D	F0	F0	F2
	DIV.D	F2	F2	F0
	L.D	F0	8(R1)	
	DIV.D	F4	F0	F6
	S.D	F4	16(R1)	
	DADDI	R1	R1	#-24
	BNEZ	R1	foo	

Clock
25

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
13	**Mul1**	Yes	div.d	R[F2]	R[F0]		
	Mul2	No					
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	Yes	bnez	R[R1]			
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24	
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26	

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 26

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
12	**Mul1**	Yes	div.d	R[F2]	R[F0]		
	Mul2	No					
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	Yes	bnez	R[R1]			
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24	
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 27

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
11	**Mul1**	Yes	div.d	R[F2]	R[F0]		
	Mul2	No					
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

...

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24	
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20		
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 38

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	Yes	sub.d	M[0+R1]			Mul1
	Add3						
	Add4						
0	**Mul1**	Yes	div.d	R[F2]	R[F0]		
	Mul2	No					
	Mul3	Yes	div.d			Mul1	Add2
	Mul4	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17		
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39	
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 39

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
5	**Add2**	Yes	sub.d	M[0+R1]	R[F2]		
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
	Mul3	Yes	div.d	R[F2]			Add2
14	**Mul4**	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40	
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39	
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0   F2
     DIV.D  F2   F2   F0
     L.D    F0   8(R1)
     DIV.D  F4   F0   F6
     S.D    F4   16(R1)
     DADDI  R1   R1   #-24
     BNEZ   R1   foo
```

Clock 40

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
4	**Add2**	Yes	sub.d	M[0+R1]	R[F2]		
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
	Mul3	Yes	div.d	R[F2]			Add2
13	**Mul4**	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

...

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39	
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock
45

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
15	**Mul3**	Yes	div.d	R[F2]	R[F0]		
8	**Mul4**	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39	
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 46

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
15	**Mul3**	Yes	div.d	R[F2]	R[F0]		
7	**Mul4**	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

...

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18		
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39	
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	Mul4
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock
53

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
15	**Mul3**	Yes	div.d	R[F2]	R[F0]		
0	**Mul4**	Yes	div.d	M[8+R1]	R[F6]		
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3	Mul4		

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18	54	
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39 – 53	54
S.D	F4	16	R1	19	20	21		
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	
Store3			
Store4			
Store5			

```
foo: L.D    F0    0(R1)
     SUB.D  F0    F0    F2
     DIV.D  F2    F2    F0
     L.D    F0    8(R1)
     DIV.D  F4    F0    F6
     S.D    F4    16(R1)
     DADDI  R1    R1    #-24
     BNEZ   R1    foo
```

Clock
54

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
14	**Mul3**	Yes	div.d	R[F2]	R[F0]		
	Mul4	No					
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3			

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18	54	
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39 – 53	54
S.D	F4	16	R1	19	20	21	55	
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	Yes	M[16+R1]	
Store3			
Store4			
Store5			

```
foo: L.D    F0    0(R1)
     SUB.D  F0    F0    F2
     DIV.D  F2    F2    F0
     L.D    F0    8(R1)
     DIV.D  F4    F0    F6
     S.D    F4    16(R1)
     DADDI  R1    R1    #-24
     BNEZ   R1    foo
```

Clock
55

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
13	**Mul3**	Yes	div.d	R[F2]	R[F0]		
	Mul4	No					
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3			

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18	54	
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39 – 53	54
S.D	F4	16	R1	19	20	21	55 – 55	56
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	No		
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 56

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
12	**Mul3**	Yes	div.d	R[F2]	R[F0]		
	Mul4	No					
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3			

...

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18	54	
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39 – 53	54
S.D	F4	16	R1	19	20	21	55 – 55	56
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	No		
Store3			
Store4			
Store5			

```
foo: L.D    F0   0(R1)
     SUB.D  F0   F0    F2
     DIV.D  F2   F2    F0
     L.D    F0   8(R1)
     DIV.D  F4   F0    F6
     S.D    F4   16(R1)
     DADDI  R1   R1    #-24
     BNEZ   R1   foo
```

Clock 68

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
0	**Mul3**	Yes	div.d	R[F2]	R[F0]		
	Mul4	No					
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi		Mul3			

Instruction		j	k	IF	ID	IS	EX	WB
L.D	F0	0	R1	1	2	3	4 – 4	5
SUB.D	F0	F0	F2	2	3	4	6 – 10	11
DIV.D	F2	F2	F0	3	4	5	24 – 38	39
L.D	F0	8	R1	4	5	6	7 – 7	8
DIV.D	F4	F0	F6	5	6	7	9 – 23	24
S.D	F4	16	R1	6	7	8	25 – 25	26
DADDI	R1	R1	#-24	7	8	9	10 – 10	12
BNEZ	R1	foo		8	9	10	13 – 13	14
L.D	F0	0	R1	14	15	16	17 – 17	18
SUB.D	F0	F0	F2	15	16	17	40 – 44	45
DIV.D	F2	F2	F0	16	17	18	54 – 68	69
L.D	F0	8	R1	17	18	19	20 – 20	21
DIV.D	F4	F0	F6	18	19	20	39 – 53	54
S.D	F4	16	R1	19	20	21	55 – 55	56
DADDI	R1	R1	#-24	20	21	22	23 – 23	25
BNEZ	R1	foo		21	22	23	26 – 26	27

	Busy	Address
Load1	No	
Load2	No	
Load3	No	
Load4	No	
Load5		

	Busy	Address	Qi
Store1	No		
Store2	No		
Store3			
Store4			
Store5			

```
foo: L.D    F0    0(R1)
     SUB.D  F0    F0    F2
     DIV.D  F2    F2    F0
     L.D    F0    8(R1)
     DIV.D  F4    F0    F6
     S.D    F4    16(R1)
     DADDI  R1    R1    #-24
     BNEZ   R1    foo
```

Clock
69

Res. Stations

Time	Name	Busy	Op	Vj	Vk	Qj	Qk
	Add1	No					
	Add2	No					
	Add3						
	Add4						
	Mul1	No					
	Mul2	No					
	Mul3	No					
	Mul4	No					
	Int1	No					
	Int2	No					
	Int3	No					
	Int4	No					
	Int5						

Reg. res.status

	F0	F2	F4	F6	R1
Qi					